Master Training: "Bootcamp : RTL, IP Integration, and SoC Signoff" at NIELIT HQ, Dwarka from 17th Dec'25 to 19th Dec'25.

DAY-1

S.No	Start Time	End Time	Title	Trainer
1	9:30 AM	10:00 AM	Opening Ceremony	Official Guest, PI and Co-PI of the project
2	10:00 AM	10:15 AM	1.1 Fundamentals of Verilog: syntax, modules, hierarchy, behavioral vs. structural modeling	**Ms. Noor Fatima Rizvi/ Mr. Mayank Singh**
3	10:15 AM	10:30 AM	1.1 Fundamentals of Verilog: syntax, modules, hierarchy, behavioral vs. structural modeling (part 2)	
4	10:30 AM	10:45 AM	Linux and VI Command Lab	
5	10:45 AM	11:00 AM	1.1 4 Bit counter	
6	11:00 AM	11:15 AM	Tea Break	
7	11:15 AM	11:30 AM	1.1 And gate	
8	11:30 AM	11:45 AM	1.1 Ripple up counter (cont.)	
9	11:45 AM	12:05 PM	1.1 verilator 4 * 1 mux	
10	12:05 PM	12:25 PM	1.1 verilator Half Adder (cont.)	
11	12:25 PM	12:40 PM	1.2 Introduction to Yosys (cont.)	
12	12:40 PM	01:00 PM	1.2 J K Flip flop	
13	01:00 PM	02:00 PM	Lunch Break	
14	02:00 PM	02:10 PM	1.2 Synthesizable vs. non-synthesizable constructs	
15	02:10 PM	02:40 PM	1.2 synth vs non-synth	
16	02:40 PM	03:00 PM	1.3 IP design methodology: specification → RTL → verification (cont.)	
17	03:00 PM	03:20 PM	1.3 UART Rx1	
18	03:20 PM	03:30 PM	1.4 IP integration at subsystem level: signal interfacing, bus protocols	
19	03:30 PM	03:45 PM	Tea Break	
20	03:45 PM	03:55 PM	1.4 IP integration at subsystem level: signal interfacing, bus protocols	
21	03:55 PM	04:20 PM	1.4 APB UART	
22	04:20 PM	04:40 PM	1.5 SoC-level considerations: clock domain, reset domain, and low-power strategies (cont.)	
23	04:40 PM	05:00 PM	1.5 UPF low power	

DAY-2

S.No	Start Time	End Time	Title	Trainer
1	09:30 AM	09:50 AM	1.6 CDC (Clock Domain Crossing) and RDC (Reset Domain Crossing) handling	**Ms. Noor Fatima Rizvi/ Mr. Mayank Singh**
2	09:50 AM	10:20 AM	1.6 Metastability without sync	
3	10:20 AM	10:40 AM	1.6 Fixing metastability using a 2 stage synchronizer	
4	10:40 AM	11:00 AM	1.7 Introduction to SoC Clocking and Reset Architectures	
5	11:00 AM	11:15 AM	Tea Break	

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6	11:15 AM	11:35 AM	1.7 clk gating	**Ms. Noor Fatima Rizvi/ Mr. Mayank Singh**
7	11:35 AM	11:55 AM	1.7 RESET Types	
8	11:55 AM	12:10 PM	1.8 Designing simple IPs (UART, GPIO, Timer, etc.)	
9	12:10 PM	12:30 PM	1.9 Integrating multiple IPs into a mini-SoC.	
10	12:30 PM	01:00 PM	1.10 Writing bus interfaces (e.g., APB, AHB-lite basic integration).	
11	01:00 PM	02:00 PM	Lunch Break	
12	02:00 PM	02:25 PM	1.11 Inserting clock/reset synchronization logic.	
13	02:25 PM	02:50 PM	1.12 Team based project collaboration using GIT	
14	02:50 PM	03:10 PM	1.13 Debugging SoC integration -Detecting a real bug	
15	03:10 PM	03:30 PM	2.1 CDC/RDC Techniques and Synchronization methodologies	
16	03:30 PM	03:45 PM	Tea Break	
17	03:45 PM	04:05 PM	2.1 Multi Stage Synchronizer for Stable CDC	
18	04:05 PM	04:25 PM	2.2 FIFO design for asynchronous Interfaces	
19	04:25 PM	04:45 PM	2.2FIFO design for asynchronous interfaces.	
20	04:45 PM	05:00 PM	2.3 Multi-clock domain architectures: clock multiplexers, clock dividers.	

DAY-3

S.No	Start Time	End Time	Title	Trainer
1	09:30 AM	10:00 AM	2.3 Multi-clock domain architectures: clock multiplexers, clock dividers- hands on	**Mr. Ankit Chaudhary / Mr. Mayank Singh**
2	10:00 AM	10:30 AM	2.4 Design techniques for low power: clock gating, power gating introduction.	
3	10:30 AM	11:00 AM	2.4 Design techniques for low power: clock gating, power gating introduction.-hands on	
4	11:00 AM	11:15 AM	Tea Break	
5	11:15 AM	11:35 AM	2.5 Understanding hierarchical design and IP reuse strategies.	
6	11:35 AM	12:00 PM	2.5 Understanding hierarchical design and IP reuse strategies.-hands on	
7	12:00 PM	12:30 PM	2.6 Reset architecture design: global, local resets, glitch-free resets.	
8	12:30 PM	01:00 PM	2.7 Building and verifying synchronizers and FIFOs.	
9	01:00 PM	02:00 PM	Lunch Break	
10	02:00 PM	02:20 PM	2.8 Clock gating implementation at RTL.	
11	02:20 PM	02:40 PM	2.9 Designing reset synchronization logic.	
12	02:40 PM	03:00 PM	2.10 Low-power Verilog coding exercises.	
13	03:00 PM	03:30 PM	2.11 Collaboratively building a multi-clock domain subsystem.	
14	03:30 PM	03:45 PM	Tea Break	
15	03:45 PM	05:00 PM	Closing ceremony	Official Guest, PI and Co-PI of the project