Session Program

Jan 9 – 15, 2026

Bootcamp: RTL, IP Integration, and SoC Signoff

Advanced SoC Architectures, CDC & Low-Power Design

Delhi, Delhi
Delhi

Sun, January 11

9:30 AM

Advanced SoC Architectures, CDC & Low-Power Design

Session | **Location:** Delhi, Delhi, Delhi | **Conveners:** Ankit Chaudhary, Mayank Singh

9:30 – 10:00 AM

2.3 Multi-clock domain architectures: clock multiplexers, clock dividers- hands on

Speaker
Ankit Chaudhary

10:00 – 10:30 AM

2.4 Design techniques for low power: clock gating, power gating introduction.

Speaker
Ankit Chaudhary

10:30 – 11:00 AM

2.4 Design techniques for low power: clock gating, power gating introduction.- hands on

Speaker
Ankit Chaudhary

11:00 AM

11:15 AM

Advanced SoC Architectures, CDC & Low-Power Design

Session | **Location:** Delhi, Delhi, Delhi | **Conveners:** Mayank Singh, Ankit Chaudhary

11:15 – 11:35 AM **2.5 Understanding hierarchical design and IP reuse strategies**

Speaker
Mayank Singh

11:35 AM – 12:00 PM

2.5 Understanding hierarchical design and IP reuse strategies.-hands on

Speaker
Mayank Singh

12:00 – 12:30 PM

2.6 Reset architecture design: global, local resets, glitch-free resets.

Speaker
Mayank Singh

12:30 – 1:00 PM **2.7 Building and verifying synchronizers and FIFOs.**

Speaker
Mayank Singh

1:00 PM

2:00 PM

Advanced SoC Architectures, CDC & Low-Power Design

Session | **Location:** Delhi, Delhi, Delhi | **Conveners:** Mayank Singh, Ankit Chaudhary

2:00 – 2:20 PM **2.8 Clock gating implementation at RTL.**

Speaker
Ankit Chaudhary

2:20 – 2:40 PM **2.9 Designing reset synchronization logic.**

Speaker
Ankit Chaudhary

2:40 – 3:00 PM **2.10 Low-power Verilog coding exercises.**

Speaker
Ankit Chaudhary

3:00 – 3:30 PM **2.11 Collaboratively building a multi-clock domain subsystem.**

Speaker
Ankit Chaudhary

3:30 PM