Session Program

Jan 9 – 15, 2026

Bootcamp: RTL, IP Integration, and SoC Signoff

RTL, IP Integration & SoC Signoff (Advanced Topics)

Delhi, Delhi
Delhi

Sat, January 10

9:30 AM

RTL, IP Integration & SoC Signoff (Advanced Topics)

Session | **Location:** Delhi, Delhi, Delhi | **Conveners:** Noor Fatima, Mayank Singh

9:30 – 9:50 AM

1.6 CDC (Clock Domain Crossing) and RDC (Reset Domain Crossing) handling

Speaker
Mayank Singh

9:50 – 10:20 AM

1.6 Metastability without sync

Speaker
Mayank Singh

10:20 – 10:40 AM

1.6 Fixing metastability using a 2 stage synchronizer

Speaker
Mayank Singh

10:40 – 11:00 AM

1.7 Introduction to SoC Clocking and Reset Architectures

Speaker
Mayank Singh

11:00 AM

11:15 AM

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11:15 – 11:35 AM

1.7 clk gating

Speaker
Noor Fatima

11:35 – 11:55 AM

1.7 RESET Types

Speaker
Noor Fatima

11:55 AM – 12:10 PM

1.8 Designing simple IPs (UART, GPIO, Timer, etc.)

Speaker
Noor Fatima

12:10 – 12:30 PM

1.9 Integrating multiple IPs into a mini-SoC.

Speaker
Noor Fatima

12:30 – 1:00 PM

1.10 Writing bus interfaces (e.g., APB, AHB-lite basic integration)

Speaker
Noor Fatima

1:00 PM

2:00 PM

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2:00 – 2:25 PM **1.11 Inserting clock/reset synchronization logic.**

Speaker
Mayank Singh

2:25 – 2:50 PM **1.12 Team based project collaboration using GIT**

Speaker
Mayank Singh

2:50 – 3:10 PM **1.13 Debugging SoC integration -Detecting a real bug**

Speaker
Mayank Singh

3:10 – 3:30 PM **2.1 CDC/RDC Techniques and Synchronization methodologies**

3:30 PM

3:45 PM

RTL, IP Integration & SoC Signoff (Advanced Topics)

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3:45 – 4:05 PM **2.1 Multi Stage Synchronizer for Stable CDC**

Speaker
Mayank Singh

4:05 – 4:25 PM **2.2 FIFO design for asynchronous Interfaces**

Speaker
Mayank Singh

4:25 – 4:45 PM **2.2FIFO design for asynchronous interfaces.**

Speaker
Mayank Singh

4:45 – 5:00 PM

2.3 Multi-clock domain architectures: clock multiplexers, clock dividers.

Speaker
Mayank Singh

5:00 PM