Session Program

Feb 2 – 6, 2026

Bootcamp: RTL , IP Integration and SoC Signoff

Verilog Fundamentals & Tool Flow

NIELIT Chitradurga, 001

Mon, February 2

9:30 AM

3:00 AM

Verilog Fundamentals & Tool Flow

Session | **Location:** NIELIT Chitradurga, 001 | **Convener:** Viswanath Naik S