Session Program

Feb 9 – 13, 2026

Bootcamp: RTL, IP Integration, and SoC Signoff

Verilog Fundamentals & Tool Flow

NIELIT Chitradurga, 001

Mon, February 9

9:30 AM
4:00 PM

Verilog Fundamentals & Tool Flow: Verilog Fundamentals & Tool Flow
Session | **Location:** NIELIT Chitradurga, 001 | **Convener:** Viswanath Naik S