Session Program

Feb 9 – 13, 2026

Bootcamp: RTL, IP Integration, and SoC Signoff

Synthesis & IP Design Basics

NIELIT Chitradurga, 001

Tue, February 10

8:00 AM

2:30 PM

Synthesis & IP Design Basics: Synthesis & IP Design Basics

Session | **Location:** NIELIT Chitradurga, 001 | **Convener:** Viswanath Naik S